Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method for fabricating a wiring structure for an integrated circuit, comprising the steps of:
forming a plurality of features in a layer of dielectric material, each of the features having sidewalls and a bottom;
forming spacers on the sidewalls;
forming conductors in the features, the conductors being separated from the sidewalls by the spacers; and
removing the spacers, thereby forming air gaps at the sidewalls so that the conductors are separated from the sidewalls by the air gaps.

[c2] A method according to claim 1, wherein said step of forming the spacers further comprises:
depositing a layer of spacer material on the sidewalls and bottom of each feature; and
removing the spacer material from the bottom using a directional etch process.

[c3] A method according to claim 1, wherein
said step of forming the conductors further comprises exposing a top surface portion of each of the spacers, and

said step of removing the spacers comprises exposing said top surface portion to an etching agent.

[c4] A method according to claim 1, wherein the features are formed using a lithography process characterized by a lithographic dimension, and the spacers are formed with a lateral dimension less than said lithographic dimension.

[c5] A method according to claim 1, wherein formation of a feature exposes a conducting stud in an underlying dielectric layer, so that formation of a conductor in said feature makes an electrical connection to the stud.

[c6] A method according to claim 1, wherein the spacers are formed with a lateral dimension greater near the bottom of the feature than near the top of the feature, so that each of the conductors is wider at a top thereof than at the bottom.

[c7] A method according to claim 1, further comprising the step of forming a second dielectric layer overlying said layer of dielectric material and the conductors, wherein the second dielectric layer has a dielectric constant less than that of said layer of dielectric material.

[c8] A wiring structure for an integrated circuit, comprising:
a first dielectric layer;

a plurality of conductors disposed on said first dielectric layer, said conductors separated laterally from each other by portions of a second dielectric layer and by air gaps, each of the conductors having air gaps adjacent thereto separating the conductor from the second dielectric layer; and

a third dielectric layer overlying the conductors,

wherein each of said conductors has a cross-section wider at a top thereof than at a bottom thereof, in accordance with each of the air gaps having a cross-section wider at a bottom thereof than at a top thereof.

[c9] A wiring structure according to claim 8, wherein said first dielectric layer and said third dielectric layer each have a dielectric constant less than that of the second dielectric layer.

[c10] A wiring structure according to claim 8, further comprising a conducting stud in said first dielectric layer and in contact with one of said conductors.

[c11] A wiring structure according to claim 9, wherein said second dielectric layer is of silicon dioxide.

[c12] A wiring structure according to claim 9, wherein a cross-section of each of said conductors has a bottom in contact with said first dielectric layer, a top in contact with

said third dielectric layer, and sides in contact only with the air gaps.